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Form PTO-1449 Modified List of Patent and Publications Cited by Applicant (Use several sheets if necessary) U.S. Department of Commerce Patent and Trademark Office		Docket No. D5116-00002A	Serial No. 092670427
		Applicant Saxena et al.	Filing Date 09/29/2000
		Group 2812	

U. S. PATENT DOCUMENTS


Examiner Initial	Cite No.	Document No.	Date	Name	Class	Subclass
MEH	AA	4,795,964	1/3/89	Mahant-Shetti et al.	324	60
MEH	AB	4,939,681	7/3/90	Yokomizo et al.	364	578
MEH	AC	5,067,101	11/19/91	Kunikiyo et al.	364	578
MEH	AD	5,068,547	11/26/91	Gascoyne	307	443
MEH	AE	5,070,469	12/3/91	Kunikyo et al.	364	578
MEH	AF	5,286,656	2/15/94	Keown et al.	324	158
MEH	AG	5,301,118	4/5/94	Heck et al.	364	468
MEH	AH	5,438,527	8/1/95	Feldbaumer et al.	364	578
MEH	AI	5,486,786	1/23/96	Lee	327	378
MEH	AJ	5,502,643	3/26/96	Fujinaga	354	488
MEH	AK	5,625,268	4/29/97	Miyanari	318	696
MEH	AL	5,627,083	5/6/97	Tounai	438	18
MEH	AM	5,629,877	5/13/97	Tamegaya	364	578
MEH	AN	5,655,110	8/5/97	Krivokapic et al.	395	500
MEH	AO	5,703,381	12/30/97	Iwasa et al.	257	48
MEH	AP	5,778,202	7/7/98	Kuroishi et al.	395	306
MEH	AQ	5,790,479	8/4/98	Conn	368	118
MEH	AR	5,798,649	8/25/98	Smayling et al.	324	551
MEH	AS	5,867,033	2/2/99	Sporck et al.	324	763
MEH	AT	5,903,012	5/11/99	Boerstler	257	48
MEH	AU	5,966,527	10/12/99	Krivokapic et al.	395	500.35

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Examiner Initial	Cite No.	OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
MEH	BF	WALTON et al., "A Novel Approach for Reducing the Area Occupied by Contact Pads on Process Control Chips", <i>Proc IEEE 1990 Int. Conference on Microelectronic Test Structures</i> , Vol. 9, March 1990, pgs. 75-80	
MEH	BG	BECKERS AND HILLTROP, "The Spidermask: A New Approach for Yield Monitoring Using Product Adaptable Tet Structures", <i>Proc IEEE 1990 Int. Conference on Microelectronic Test Structures</i> , Vol. 8, March 1990, pgs. 61-66	
MEH	BH	LIEBMAN et al. "Understanding Across Chip Line Width Variation: The First Step Toward Optical Proximity Correction", <i>SPIE Vol. 3051</i> , pgs.124-136.	
MEH	BI	PCT International Search Report, March 13, 2001	
MEH	BJ	CONTI. M. et al., Parametric Yield Formulation of MOS IC's Affected by Mismatch Effect. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , May 1999, Vol. 18, No. 5, Pages 582-596	
MEH	BK	TO. H. et al., Mismatch Modeling and Characterization of Bipolar Transistors for Statistical CAD. <i>IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications</i> , July 1996, Vol. 43, No. 7, Pages 608-610	
MEH	BL	FELT. E. et al., Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's, 1994 <i>IEEE/ACM International Conference on Computer-Aided Design</i> , November 1994, Pages 272-277	
MEH	BM	MICHAEL. C. et al., A flexible Statistical Model for CAD of Submicrometer Analog CMOS Integrated Circuits, 1993, <i>IEEE/ACM International Conference on Computer-Aided Design</i> , November 1993, Pages 330-333	
MEH	BN	OGRENCI. A. et al., Incorporating MOS Transistor Mismatches Into Training of Analog Neural Networks, <i>Proceedings of NC, International ICSC/IFAC Symposium on Neural Computation</i> , September 1998, Abstract only	
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